OSTİM TECHNICAL UNIVERSITY
INSTITUTE OF SCIENCES
ELECTRICAL & ELECTRONICS ENGINEERING
COURSE SYLLABUS
2022-2023 FALL

EEE303 Digital System Design							
Course Name	**Code**	**Semester**	**Theory (hour/week)**	**Application (hour/week)**	**Lab (hour/week)**	**Credits**	**ECTS**
Digital System Design	EEE303	Fall	3	0	0	3	4

Course Language	English
Course Type	Compulsory
Course Level	Undergraduate
Mode of Delivery	In class lectures
Course Lecturer(s)	Dr. Hüseyin KÖSE
Teaching Methods and Techniques of the Course	Lectures, Homeworks

Course Objectives

The objective of this course is to learn the operation principles of gate array logic circuits and how to program to gate array logic circuits. Understand and clarify the differences between microcontroller programming and VHDL

Learning Outcomes

Having successfully completed this course, students will be able to:
LO-1: Understand the concept of gate array logic circuits and field programmable gate array logic circuits.
LO-2: Can identify the basic gate array logic circuits and can design complex electronic circuit elements like shift register, memory, level shifter etc.
LO-3: Can design gate array logic circuits to solve any basic mathematical or logical problems.
LO-4: Can understand the working principles of serial and parallel communication requirements, hardware and protocol types.
LO-5: Know the history of programming languages (ASM, Basic, C, C++, etc.) and Understand the Hardware Programming Language VHDL.

Course Description

Basic characteristics and operation principles of gate array logic circuits. Computer working principle. Memory organizations. Serial and Parallel data transfers, communication types, hardwares and protocols. Microcontroller, microprocessor and FPGA architecture and working principles. Introduction to FPGA designing and VHDL programming.

Subjects and Related Preparation Studies	
Week	**Subjects**
1	Remembering of Logic Gates and Boolean Mathematics, Encoders, Decoders and Multiplexers
2	Counters
3	Registers
4	Memory and Programmable Logic, PAL, PLA
5	Register Transfer Level
6	Computer Architecture and Mathematics
7	CPU and Basic Program Instructions
8	Field Programmable Gate Array Logics (FPGA) and design principles
10	**Midterm**
11	Input Output Organizations, Memory Organizations
12	Transistor-Transistor Logic Circuits
13	Designing Combinational Logic Circuits, CMOS input output port designing
14	Microcontroller, Microprocessor and FPGA Architectures and Design Principles
15	Microprocessor Programming, FPGA designing and VHDL Programming
16	**Final Exam**

Course Notes/Textbooks

1. Lecture Notes and Presentations
2. Digital Design 5th, Ed. with an Introduction to the Verilog HDL (fifth edition), M. Morris Mano, Michael D. Ciletti

Evaluation System		
Semester Activities	**Number**	**Weighting**
Participation		
Laboratory		
Application		
Field Work		
Portfolio		
Quizzes / Studio Critiques		
Homework / Assignments	1	20%
Presentation		
Project		
Report		
Seminar		
Midterm	1	40%
Final	1	40%
	Sum	**100 %**
Weighting of Semester Activities on the Final Grade		60 %
Weighting of End-of-Semester Activities on the Final Grade		40 %
	Sum	**100 %**

Course Category	
Core Courses	x
Major Area Courses	x
Supportive Courses	x
Media and Management Skills Courses	
Transferable Skill Courses	x

Course Learning Outcomes and Program Qualifications Relationship						
No	**Program Competencies/Outcomes**	**Contribution Level**				
		1	**2**	**3**	**4**	**5**
1	Ability to apply knowledge of mathematics, science, and engineering				x	
2	Ability to design and conduct experiments and to analyze and interpret experimental results.				x	
3	Ability to design a system, component, and process according to specified requirements.					x
4	Ability to work in teams in interdisciplinary areas.					x
5	Ability to identify, formulate and solve engineering problems.					x
6	Identifies, defines, formulates and solves complex network problems; chooses and applies analysis and modeling methods suitable for this purpose.				x	
7	Develops, selects and uses modern techniques and tools necessary for the analysis and solution of complex problems encountered in Electrical and Electronics Engineering applications; uses required technologies effectively.					x

ECTS / Workload Table			
Semester Activities	**Number**	**Duration (Hours)**	**Workload**
Theoretical Course Hours (Including exam week: 16 x total hours)	16	3	48
Laboratory			
Application			
Portfolio			
Field Work			
Study Hours Out of Class			
Presentation			
Project			
Reports			
Homework/Assignments	1	20	20
Quizzes / Studio Critiques			
Midterms	1	20	20
Final Exam	1	20	20
Total	**(ECTS 108/25 = 4.32)**		**108**